

AFRL CALL FOR DAGSI Topics

1. Research Title: *Hardware Acceleration of Assessment Tools and Techniques for Trusted Microelectronics*

2. Individual Sponsor:

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3. Academic Area and Education Level: Electrical & Computer Engineering or Computer Science /FPGA, OpenCL, Verilog, VHDL (Ph.D. or M.S. Level)

4. Objectives: The primary objective of this research is to decrease the Time and Expertise Required to Assess (TERA) gate level Integrated Circuit designs for the presence of hardware Trojans or malicious modifications through the reduction of algorithm run time via hardware in the loop acceleration. This research will include the modification of existing and the development of new logic comparison algorithms targeted to operate on Field Programmable Gate Arrays (FPGAs). This research may be implemented using an OpenCL framework or through a Hardware Description Language (HDL) such Verilog or VHDL. While the primary focus is on hardware acceleration of existing algorithms, other areas of emphasis will include the overall framework integration for hardware acceleration, data formatting for efficient transferring both to and from hardware, and software/hardware hybrid algorithm development to explore rapid investigation of novel hardware accelerated validation approaches.

5. Description: A dramatic drop of Integrated Circuit (IC) production in the United States has led to a shifting of state of the art fabrication facilities overseas. As it is desirable for the DoD to maintain access to these manufacturing capabilities, the risk of design modification when using untrusted fabrication facilities must be reduced. Key to mitigate the increased susceptibility to Trojans or malicious modifications inserted during untrusted fabrication are analysis techniques to detect insertions. However, traditional detection techniques suffer from scalability issues as they are intended for the forward flow of IC design/manufacturing process. While new methods have been developed to fill in the gaps left by traditional tools, the analysis time is still unacceptable due to the exponential increase in state space as design size increases. The incorporation of hardware acceleration in the analysis of ICs to detect malicious modifications will prove to be an invaluable capability for ensuring the safety of our electronic systems.

6. Research Classification/Restrictions: This work is unclassified; U.S. Citizens only.

7. Eligible Research Institutions:

X Universities (DAGSI) _ AFIT only _ USAF A