RY19-18

AFRL CALL FOR DAGSI Topics

1. Research Title: *Image Alignment and Data Fusion for Trusted Microelectronics*

2. Individual Sponsor:

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3. Academic Area and Education Level: Electrical & Computer Engineering/Mixed-Signal and Formal Verification/Microscopy (Ph.D. Level)

4. Objectives: The primary objective of this research is to develop methods of data fusion and alignment (temporal and spatial) using multiple imaging modalities gathered from integrated circuit (IC) test articles. The aggregated image library will be utilized to verify an IC is an exact production (a "trusted" device with nothing extra and nothing missing) of an intended design. For example, a composite image formed via a mosaic of scanning electron microscope (SEM) images contains high-fidelity detail of an IC's internal structure but time to complete and the destructive nature of such an image prevents wide-spread utilization as a trust verification tool. Electromagnetic (EM) scanning, or thermal emissions, can be completed in less time but may not provide required fidelity. The aggregation effort seeks to improve the utility of rapid image techniques by associating signatures in the lower fidelity domain to items of interest typically only observed with more costly techniques resulting in tailorable verification methods. For example, lower risk components may solely use low fidelity images tied with varying confidence to features observable with higher cost methods. Additionally, correlated low fidelity images may identify areas that need additional imaging rather than conducting an initial scan with a high cost technique across the entire IC.

5. Description: As microelectronics continues to advance in their complexity and to be purchased from varied supply chains, there is an increased concern of integrated circuits containing hardware Trojans (malicious bugs) or fabrication faults that would compromise the integrity of the original chip functionality. As a result, there is an increasing concern regarding the level of trust one can have in the fabricated chip once it has been received back from the foundry, namely if the chip is fully equivalent to the original design without additional, degraded, or auxiliary functionality. The varied and sometimes unknown supply chain presents many opportunistic points in the manufacturing flow for Trojan insertion. Current formal verification and fault analysis techniques primary focus on confirming correct function and performance but do not look for extra functionality even though such capability exits. The scope of the trusted microelectronics research involves developing methods to combine fault analysis tools and techniques to provide cost effective and rapid verification of "trust" - correctly manufactured microelectronics.

6. Research Classification/Restrictions: This work is unclassified; U.S. Citizens only.

7. Eligible Research Institutions:

X Universities (DAGSI) _ AFIT only _ USAF A